IN THE SPECIFICATION

Please replace paragraph [0004] as follows:

A double gate (DG) device, such as shown in Figures 2A and 2B, have been proposed to alleviate the silicon thickness issue. The double gate (DG) device 200 includes a silicon body 202 formed on an insulating substrate 204. A gate dielectric 206 is formed on two sides of the silicon body 202 and a polysilicon gate electrode 208 is formed adjacent to the gate dielectric 206 formed on the two sides of the silicon body 202. A sufficiently thick insulating layer 209, such as silicon nitride, electrically isolates the gate electrode 208 from the top of silicon body 202. Double gate (DG) device 200 essentially has two gates, one on either side of the channel of the device. Because the double gate device 200 has a gate on each side of the channel, thickness ~~(Tsi)~~ (T_{si}) of the silicon body can be double that of a single gate device and still obtain a fully depleted transistor operation. That is, with a double gate device 200 a fully depleted transistor can be formed where ~~Tsi~~ T_{si} = (2xLg)/3. The most manufacturable form of the double gate (DG) device 200, however, requires that the body 202 patterning be done with photolithography that is 0.7 x smaller than that used to pattern the gate length (Lg) of the device. In order to obtain high density integrated circuits, it is generally desirable to have the most aggressive lithography occur with respect to the gate length (Lg) of the gate electrode 208. Although, double gate structures double the thickness of the silicon film (since there now is a gate on either side of the channel) these structures, however, are hideously difficult to fabricate. For example, silicon body 202 requires a silicon body etch which can produce a silicon body 202 with an aspect ratio (height to width) of about 5:1.